3.1 First, the cost per wafer for each step and scan. 248nm – number of wafers for four years = 4*365*24*80 = 2,803,200. 193nm = 4*365*24*20 = 700,800. The cost per wafer is the (equipment cost)/(number of wafers) which is for 248nm $10M/ 2,803,200 = $3.56 and for 193nm is $40M/700,800 = $57.08. For a run through the equipment 10 times per completed wafer is $35.60 and $570.77 respectively.

Now for gross die per wafer. For a 300mm diameter wafer the area is roughly 70,650 mm^2 ($\pi*(r^2/A - r/(\text{sqrt}(2*A))$). For a $50mm^2$ die in 90nm, there are 1366 gross die per wafer. Now for the tricky part (which was unspecified in the question and could cause confusion). What is the area of the 50nm chip? The area of the core will shrink by $(90/50)^2 = .3086$. The best case is if the whole die shrinks by this factor. The shrunk die size is $50*.3086 = 15.43mm^2$. This yields 4495 gross die per wafer.

The cost per chip is $35.60/1413 = $0.026 and $570.77/4578 = $0.127 respectively for 90nm and 50nm. So roughly speaking, it costs $0.10 per chip more at the 50nm node.

Obviously, there can be variations here. Another way of estimating the reduced die size is to estimate the pad area (if it's not specified as in this exercise) and take that out or the equation for the shrunk die size. A $50mm^2$ chip is roughly 7mm on a side (assuming a square die). The I/O pad ring can be (approximately) between 0.5 and 1 mm per side. So the core area might range from $25mm^2$ to $36mm^2$. When shrunk, this core area might vary from 7.7 to $11.1mm^2$ (2.77 and 3.33mm on a side respectively). Adding the pads back in (they don't scale very much), we get die sizes of 4.77 and 4.33 mm on a side. This yield possible areas of 18.7 to 22.8 mm^2, which in turn yields a cost of processing on the stepper of between $0.155 and $0.189. This is a rather more pessimistic (but realistic) value.

3.3 Polycide – only gate electrode treated with a refractory metal. Salicide – gate and source and drain are treated. The salicide should have higher performance as the resistance of source and drain regions should be lower. (Especially true at RF and for analog functions).

transistor-masks

~ Weste Harris chapter 3 extra problem

From a designer's point of view, what combination of basic masks combine together to make a N-MOS transistor?

- Functional layers:
    - n-diff
    - poly
- Fabrication masks:
    - active
    - n-select
    - poly

Which ones are used for a P-MOS transistor?

- Functional layers:
    - n-well
    - p-diff
    - poly
- Fabrication masks:
    - n-well
    - active
    - p-select
    - poly