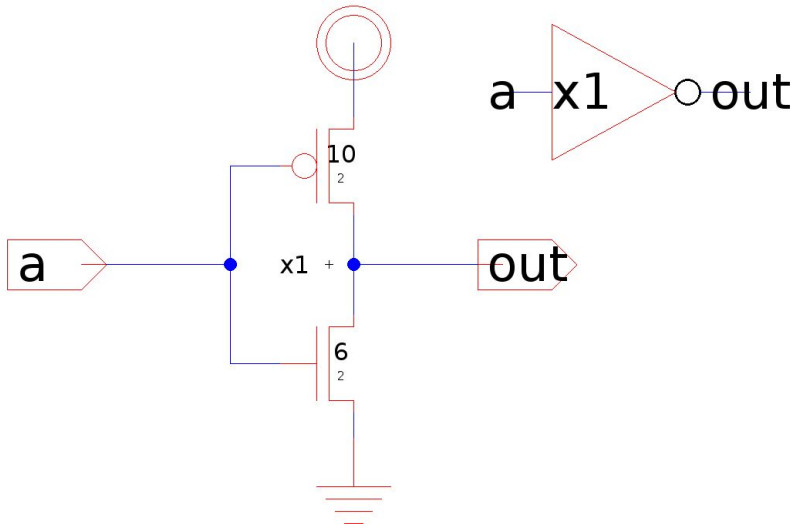
hw07-solution

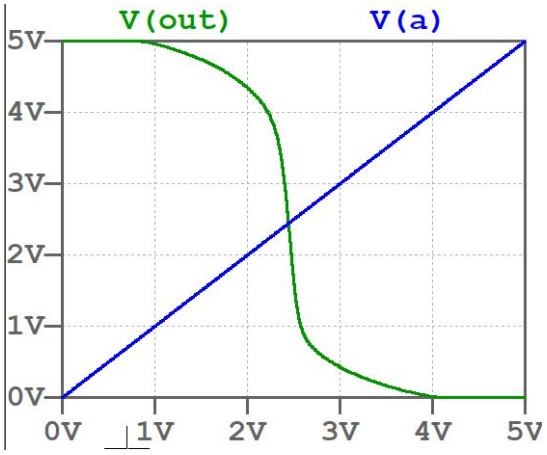
2020 Dan White

The JELIB for this is available by request.

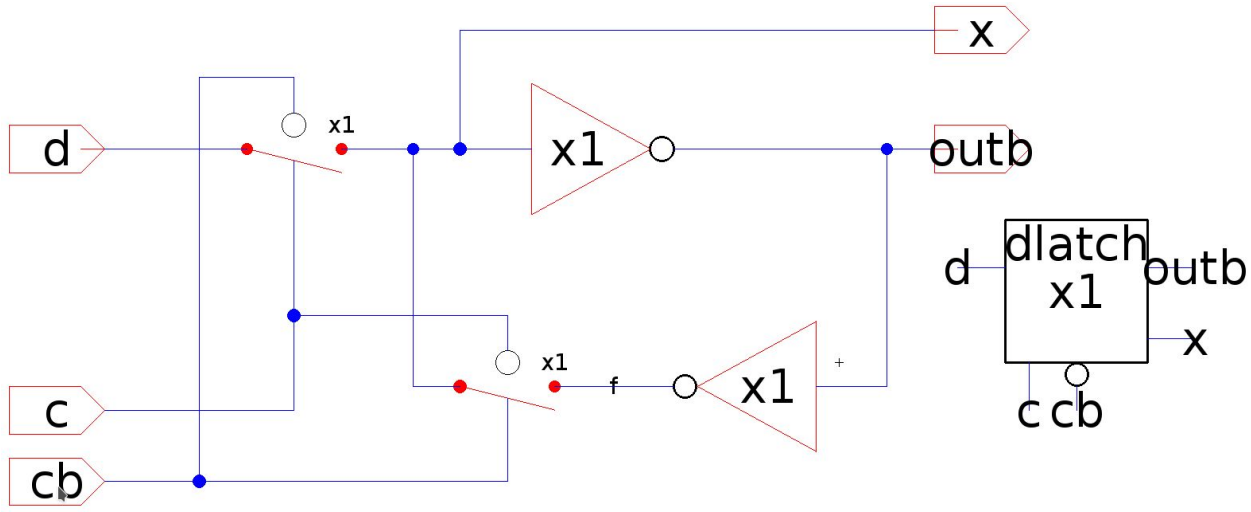
inv-x1



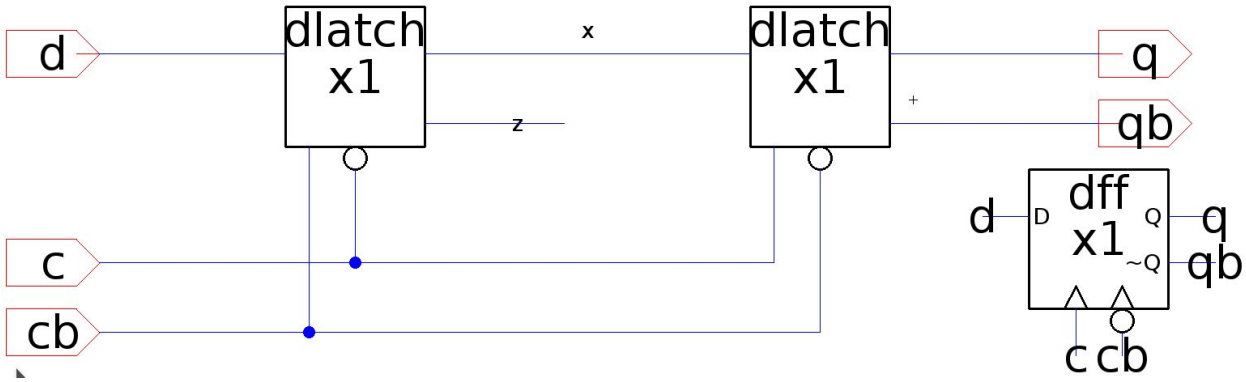
Voltage Transfer Curve



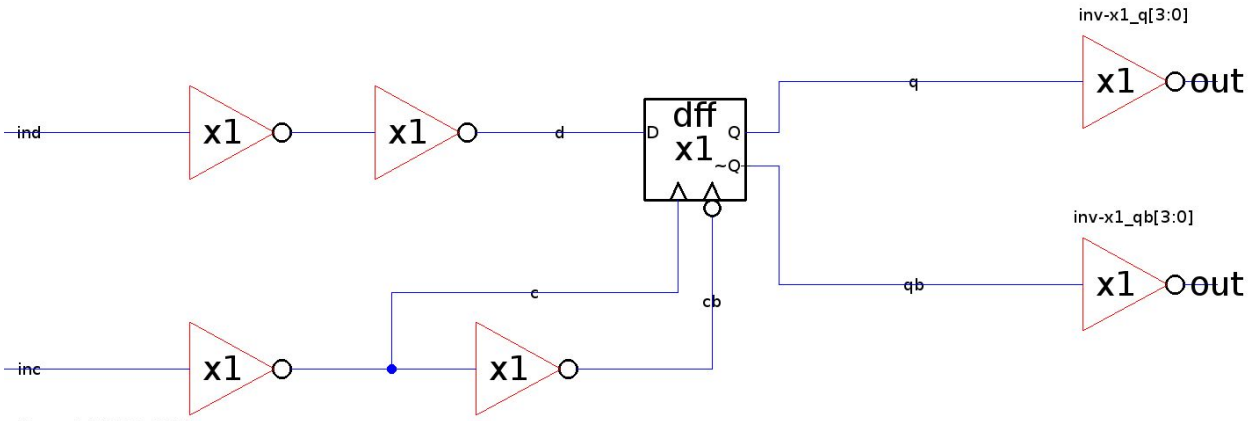
D latch


x
d
x1
x1
outb
c
cb
x1
f
x1
dlatch
x1
d
outb
x
c cb

DFF


d
dlatch
x1
x
z
dlatch
x1
q
qb
c
cb
dff
x1
d
D
Q
~Q
q
qb
c cb

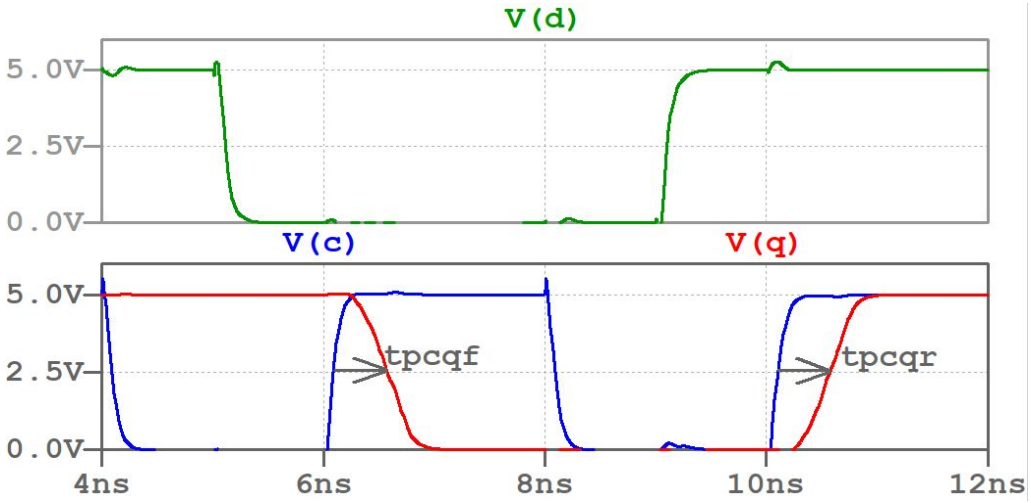
DFF test bench schematic




```
Vsupply VDD 0 DC 5
Vck inc 0 DC 0 PULSE 0 5 0 10p 10p 3n 6n
Vd ind 0 DC 0 PULSE 5 0 200p 10p 10p 3n 5.99n
.include c5.txt
.tran 2000n UIC
.save v(d) v(c) v(cb) v(q) v(qb) dialogbox
*.options post
```

tpcqr and tpcqf simulations

```
Vsupply VDD 0 DC 5
Vck inc 0 DC 0 PULSE 0 5  0 10p 10p 2n 4n
Vd  ind 0 DC 0 PULSE 0 5 1n 10p 10p 4n 8n
.include c5.txt
.tran 20n
.save v(d) v(c) v(cb) v(q) v(qb)

.meas tran tpcqf trig v(c)=2.5 rise=2 targ v(q)=2.5 fall=1
.meas tran tpcqr trig v(c)=2.5 rise=3 targ v(q)=2.5 rise=1

* error log output:
* tpcqf=4.86942e-10 FROM 6.08499e-09 TO 6.57193e-09
* tpcqr=4.66708e-10 FROM 1.00984e-08 TO 1.05651e-08
*
* tpcqr = 487ps
* tpcqf = 467ps
```



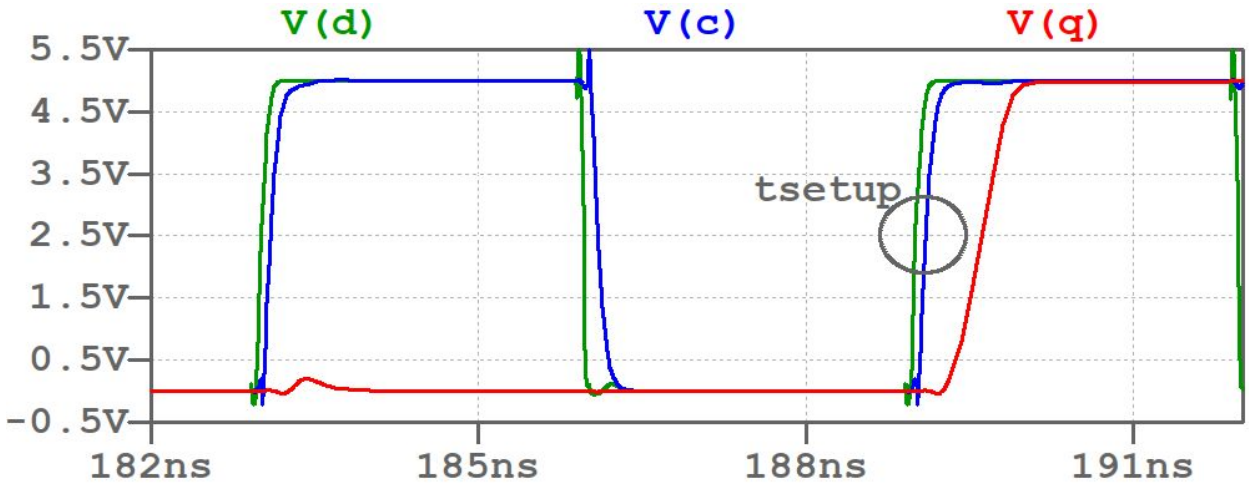
Setup time simulations

There are **two**: Capturing D → high and D → low.

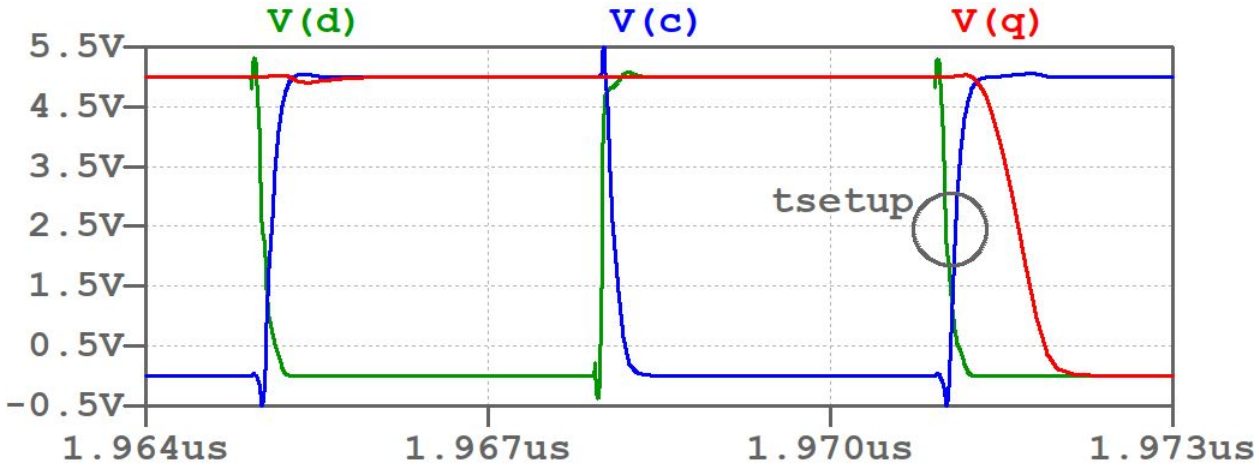
Longest setup time is 92ps. Use this as the DFF's metric since we want it to work for *both* logic levels.

```
Vsupply VDD 0 DC 5
Vck inc 0 DC 0 PULSE 0 5 0 10p 10p 3n 6n
Vd ind 0 DC 0 PULSE 5 0 200p 10p 10p 3n 5.99n
.include c5.txt
.tran 2000n
.save v(d) v(c) v(q)

* rise= and fall= parameters need to be changed
* match FROM and TO times to the cycles to measure!
.meas tran tsetuph trig v(d)=2.5 rise=32 targ v(c)=2.5 rise=32
.meas tran tsetupl trig v(d)=2.5 fall=330 targ v(c)=2.5 rise=329

* log result:
* tsetuph=9.16841e-11 FROM 1.88996e-07 TO 1.89087e-07
* tsetupl=8.45364e-11 FROM 1.97101e-06 TO 1.97109e-06
```

tsetup high = 92ps



tsetup low = 85ps



Simulation notes

The clock input source has a period of 6.00ns, while the D input source has a period of 5.99ns. At each cycle of the clock, the D input will be 10ps *earlier* than it was the previous cycle.

The way the clock buffer is setup adds an inversion between the SPICE source and the probed clock node at the input to the DFF.

The D source is delayed by 200ps. This means at the first rising clock edge of the simulation around 3ns, the D input will rise about 190ps **after** the clock. In these first clock edges, the D input is therefore **low** at the clock edge and Q remains low also.

At each clock cycle, the D input gets 10ps earlier in time with respect to the clock. Eventually the D input will change **before** the clock edge and early enough for the DFF to transfer a **high** to the Q output.

By definition, the closest time that D can change before the clock edge is the **minimum setup time**.

Setup time, as an unqualified measurement, is a little ambiguous. It merely means the time that D is stable before the clock edge. We are actually interested in the **minimum** time that D needs to be stable before the clock edge.

Therefore **minimum setup time** is the better term to use when discussing what we just estimated. Note the language! You can *estimate* the minimum setup time, but it is not a quantity that can be directly *measured*, only inferred by observing a setup time failure and a setup time success. The "true" minimum setup time is **somewhere between** those two D → CLK times.