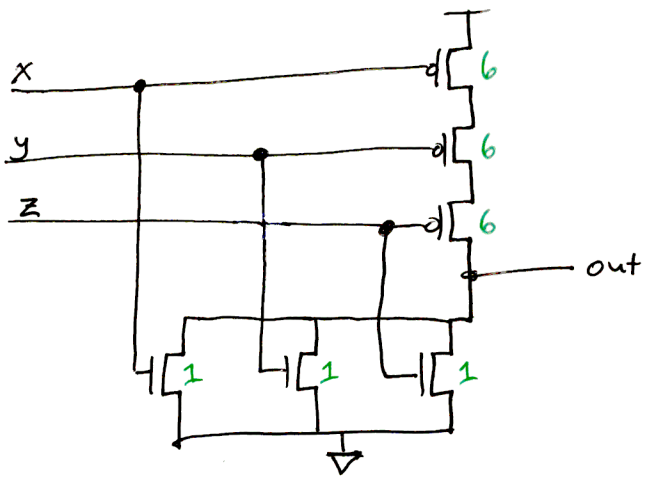
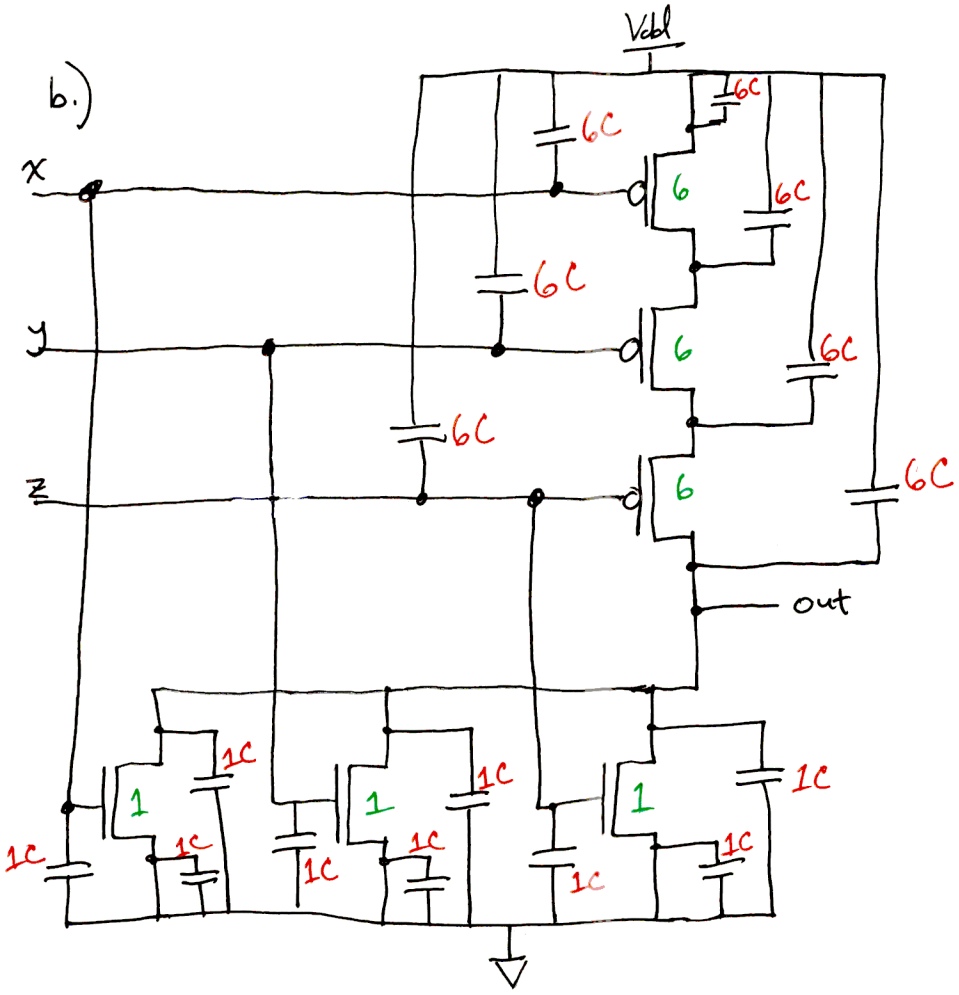
3-input CMOS NOR gate

Similar progression as Weste + Harris Figure 4.7

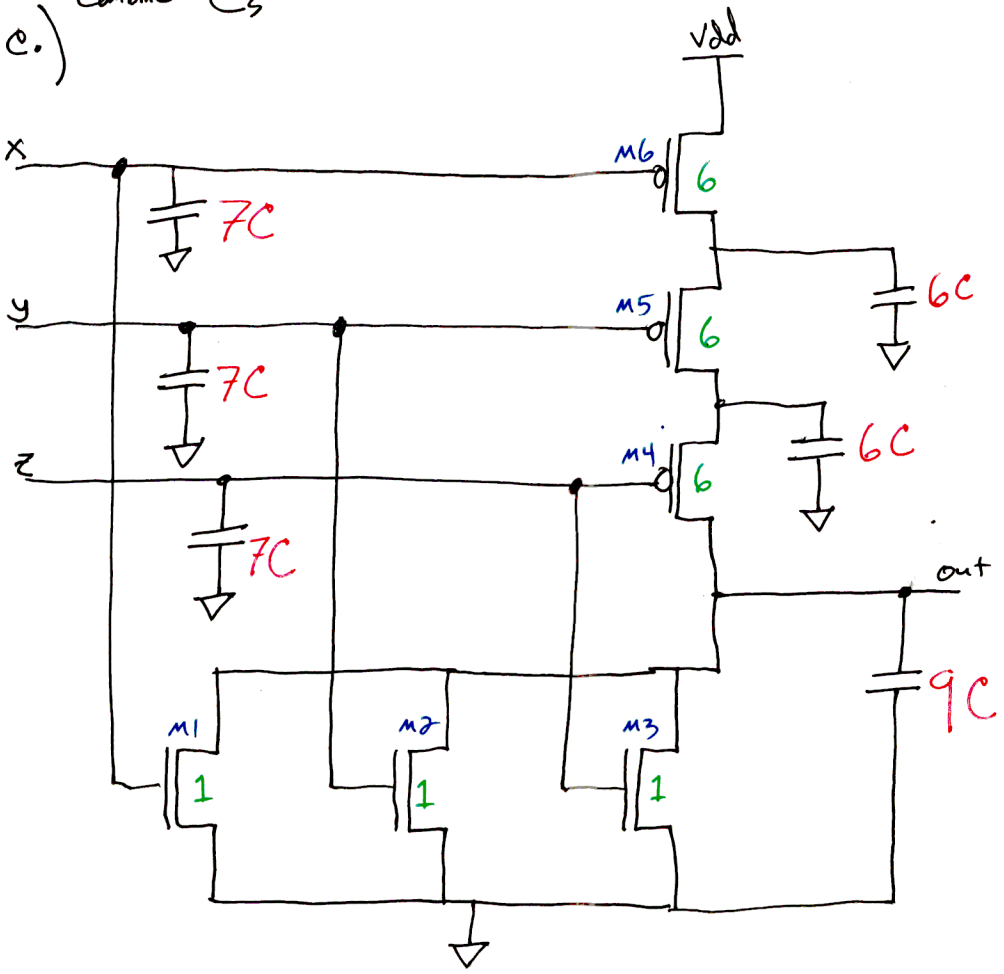
a.)



b.)

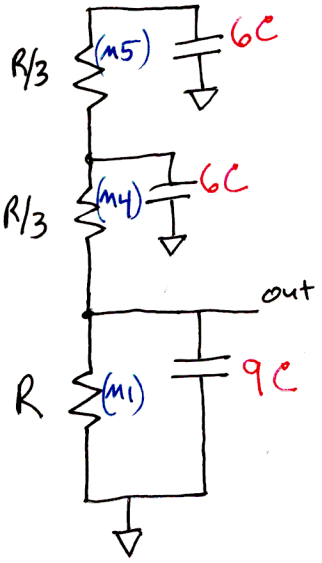


c.) Combine C's



d) Falling worst-case

→ all C's start charged to Vdd



e.) Rising worst-case

→ all C's start discharged