westeharris_p4.11-solution

4.11 Consider four designs of a 6-input AND gate shown in Figure 4.40. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for $H = 1$? For $H = 5$? For $H = 20$? Explain your conclusions intuitively.

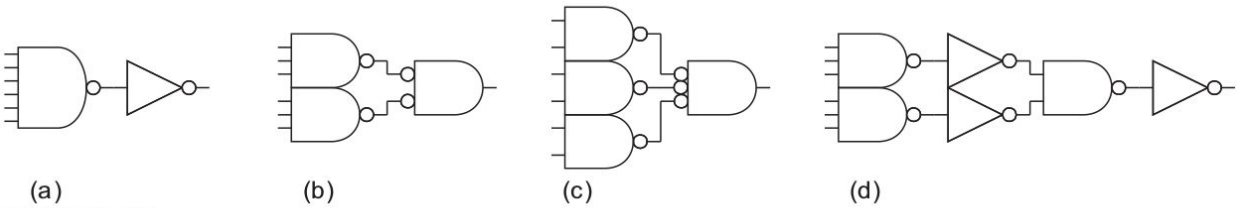

FIGURE 4.40 6-input AND gate

4.11 $D = N(GH)^{1/N} + P$. Compare in a spreadsheet. Design (b) is fastest for $H = 1$ or 5. Design (d) is fastest for $H = 20$ because it has a lower logical effort and more stages to drive the large path effort. (c) is always worse than (b) because it has greater logical effort, all else being equal.

Comparison of 6-input AND gates

Design	G	P	N	D (H=1)	D (H=5)	D (H=20)
(a)	**8/3 * 1**	**6 + 1**	**2**	**10.3**	**14.3**	**21.6**
(b)	**5/3 * 5/3**	**3 + 2**	**2**	**8.3**	**12.5**	**19.9**
(c)	**4/3 * 7/3**	**2 + 3**	**2**	**8.5**	**12.9**	**20.8**
(d)	**5/3 * 1 * 4/3 * 1**	**3 + 1 + 2 + 1**	**4**	**11.8**	**14.3**	**17.3**