Dan White

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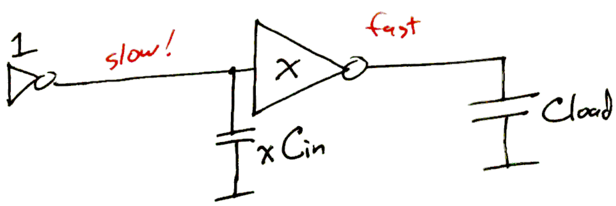
Sizing a Chain of inverters

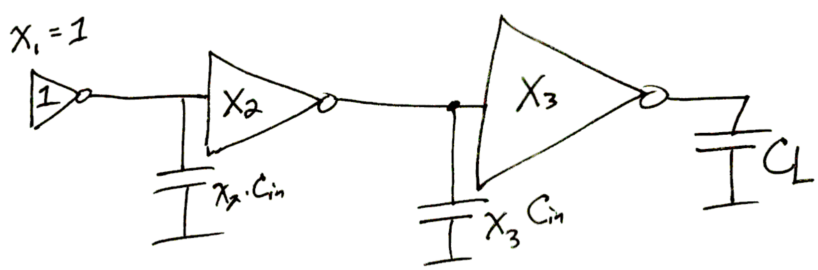
Problem: a logic signal needs to drive a large load (Cload), such as bringing a signal off chip to a circuit board.

Inverter (base size) is small → R_{out} is large, C_{in} is large, so delay is <u>really long</u>. $(R_{out} \cdot C_{load})$

Use a large (transistor width) inverter!
But <u>something</u> needs to drive this inverter's (now large) input C_{in}.

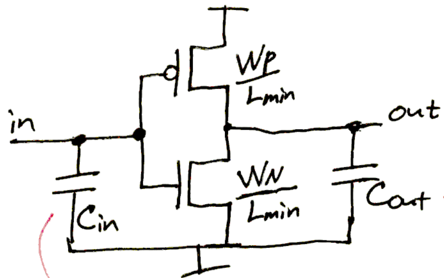


So, use a not so large inverter do drive the large one

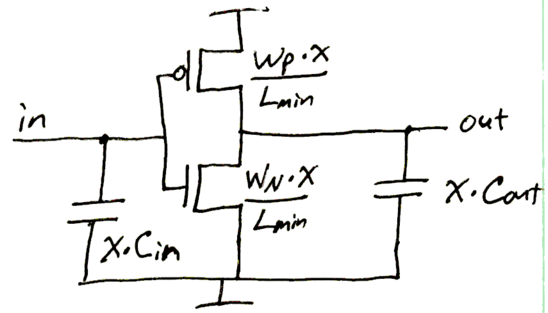


?: How many stages to use and how to choose the x_i's?
↳ this is an optimization problem

Base-sized inverter



Larger drive strength inverter



usually $W_P \approx 2 \cdot W_N$

so ON resistances / drive strengths are about the same

$$R_N \approx R_P = R$$

$$R_{drive} = \frac{R}{X}$$

$$C_{inx} = X \cdot C_{in}$$

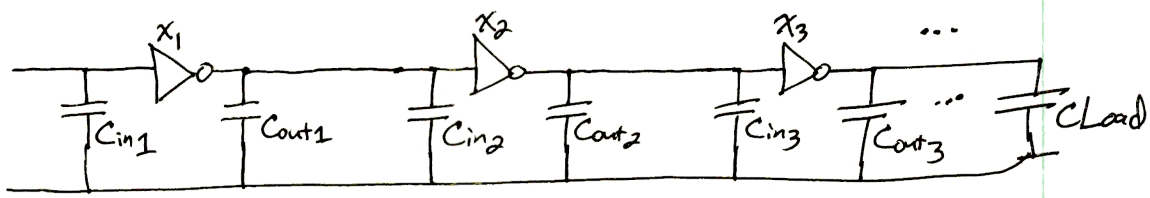
$$C_{out\,x} = X \cdot C_{out}$$

Inverter delay

$$d = (\text{constant}) \cdot \frac{R}{X}\left(X \cdot C_{out} + C_{load} \right)$$

$$= (\text{constant}) \left(\underbrace{R \cdot C_{out}}_{\text{parasitic constant!}} + \underbrace{\frac{R \cdot C_{load}}{X}}_{\text{due to load}} \right)$$

base value



$$\text{Total delay} = \sum_{i=1}^{N} \left(R \cdot C_{out} + \frac{R \cdot X_{i+1} \cdot C_{in}}{X_i} \right)$$

base

★ $\boxed{\text{parameter } \gamma = \frac{C_{out\ base}}{C_{in\ base}}}$

$$\text{Total delay} = \sum_{i=1}^{N} \left(R \cdot C_{out} + \frac{R \cdot C_{out} \cdot X_{i+1}}{\gamma \cdot X_i} \right)$$

$$\text{total delay} = N \cdot R \cdot C_{out} \sum_{i=1}^{N} \left(1 + \frac{x_{i+1}}{\gamma x_i}\right) = \underbrace{N \cdot R \cdot C_{out} \sum_{i=1}^{N} \left(1 + \frac{Cin_{i+1}}{Cin_i}\right)}$$

remember: $Cin_N = C_{load}$ (only $N-1$ unknowns)

$$\frac{x_{i+1}}{x_i} = \frac{Cin_{i+1}}{\underbrace{Cin_i}}$$ more useful term for non-inverters

Minimize total delay by taking $N-1$ partial derivatives and making all $= \phi$.

$$\frac{\partial}{\partial Cin_j}\left(\text{total delay}\right) = \phi \qquad \text{for } j = [1 \dots N-1]$$

→ expand the series to see this pattern.

$$\cdots \overbrace{\left(1 + \frac{Cin_{j-1+1}}{\gamma Cin_{j-1}}\right)}^{j-1} + \overbrace{\left(1 + \frac{Cin_{j+1}}{\gamma Cin_j}\right)}^{j} + \overbrace{\left(1 + \frac{Cin_{j+1+1}}{\gamma Cin_{j+1}}\right)}^{j+1}$$

only these terms stay with $\frac{\partial}{\partial Cin_j}$ derivative

$$\frac{\partial}{\partial Cin_j}\left(\frac{Cin_j}{\gamma Cin_{j-1}} + \frac{Cin_{j+1}}{\gamma Cin_j}\right) = \underbrace{\frac{1}{\gamma Cin_{j-1}} - \frac{Cin_{j+1}}{\gamma (Cin_j)^2} = \phi}_{☆}$$

solution is/are

$$\frac{1}{\gamma Cin_{j-1}} = \frac{Cin_{j+1}}{\gamma (Cin_j)^2} \qquad Cin_j = \sqrt{Cin_{j-1} \cdot Cin_{j+1}} \quad \underline{\text{geometric mean}} \; ☆$$

$$\Downarrow$$

$$\underbrace{\frac{Cin_j}{Cin_{j-1}}}_{f_{j-1}} = \underbrace{\frac{Cin_{j+1}}{Cin_j}}_{f_j} \Longrightarrow \boxed{\text{all } f_j\text{'s must be equal}}$$

$C_{in_{(N-1)+1}} = C_{load}$ last capacitor is the load

$$\frac{C_{load}}{C_{in_1}} = f_1 \cdot f_2 \cdots f_N = f^N = F \qquad = G H$$

all 1 for inverters

now we can write:

$$\text{total delay} = R \cdot C_{out} \cdot N \cdot \left(1 + \frac{f}{\gamma}\right)$$

and $N = \dfrac{\ln F}{\ln f}$

$$\text{total delay} = R \cdot C_{out} \cdot \frac{\ln F}{\ln f}\left(1 + \frac{f}{\gamma}\right)$$

what is the best f? $\rightarrow$ derivative $= \phi$!

$$\frac{d}{df}(\text{total delay}) \overset{R \cdot C_{out}}{=} \frac{d}{df}\left(\frac{\ln F}{\gamma}\left(\frac{\gamma}{\ln f} + \frac{f}{\ln f}\right)\right)$$

$$= R \cdot C_{out} \frac{\ln F}{\gamma}\underbrace{\left[\frac{-\gamma}{f \cdot \ln^2(f)} + \frac{\ln(f) - 1}{\ln^2(f)}\right]}_{} = \phi$$

$$-\gamma/f + \ln(f) - 1 = \phi$$

$$\ln f = 1 + \frac{\gamma}{f}$$

$$f_{opt} = \exp\left(1 + \frac{\gamma}{f_{opt}}\right)$$

no closed-form solution unless $\gamma = \phi$:(

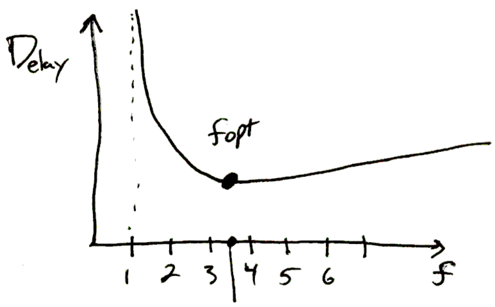
$$\gamma = f(\ln f - 1) \longleftarrow$$ plot this and swap the axes!

Find f for a few values of γ:

γ	f_{opt}
ϕ	2.72 $(=e)$
1	3.59
2	4.32

⟵ most processes have $\frac{C_{out}}{C_{in}} = \gamma \approx 1$

plot total delay vs. f (for $\gamma = 1$)



$$N_{opt} = \frac{\ln F}{\ln f_{opt}}$$

$$f_{opt} = F^{1/N_{opt}}$$

Observations about this plot:

- Choosing f smaller than f_{opt}: more stages (more area and power) ☹
  increasing delay ☹
- Choosing f larger than f_{opt}: less stages less area and power ☺
  not much delay increase 😐

⟹ Usually, round to a smaller N
and use a larger f

☆☆☆ This is the origin of "fan-out of 4", or stage effort $f = 4$
as a good rule-of-thumb

Logical Effort terminology

(sometimes N needs to be even or odd for
logic function purposes)

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